RF Energy Harvesting Circuits

Joseph Record*

University of Maine

ECE–547

Fall 2011

Abstract

This project presents the design and simulation of various energy harvester circuits. The overall design consists of six different "voltage doubler" configurations. From the six configurations, 14 independent energy harvester circuits have been designed, each consisting of various series connections of the voltage doublers. Multiple RF harvesters were designed to determine the effect of component value and size. The cascaded voltage doulber circuits rectify the full-wave peak-to-peak voltage of an incoming RF signal to produce a DC voltage, ideal for low power sensors networks or other embedded devices. Simulations with a 150 mV 90 MHz input signal indicate an average output voltage of approximately 1.75 V over a 100 μs time scale for 20 cascaded voltage doublers. This corresponds to a gain of roughly 11.5 V/V. Cascading more voltage doublers is shown to increase this gain. Test and verification procedures are outlined and described.

*http://www.eece.maine.edu/vlsi/2011/Record/

Contents

List of Figures

1 Introduction

There has been a recent proliferation of sensors and other embedded devices in recent years. These devices are used for a wide range of applications, from the sensing of gases, to shellfish toxins, to monitoring building structure. With the growth of these sensor networks, there is a need for a novel means of powering said devices. Radio frequency energy harvesting is one such method. With RF energy harvesting, ambient radio waves from cellular towers are rectified via a Schottky diode. The resulting charge is stored in a capacitve element. By cascading a series of these elements, an RF input signal captured with an antenna can be converted to a significantly higher DC voltage which a sensor can then use. This means that sensor batteries need not be replaced, saving time and money as well as increasing sensor network reliability.

The overall chip design consists of six different "voltage doubler" configurations. Each voltage doubler consists of two Schottky diodes — either n-type or p-type — and two capcitors. From the six configurations, 14 independent energy harvester circuits have been designed, each consisting of various series connections of the voltage doublers. Each of the energy harvesters are three terminal devices, with a ground, RF input, and a DC output.

This report describes the theory, implementation, and verification of these energy harvester devices.

2 Analysis

The circuit theory behind each voltage doubler is relatively simple. Each doubler consists of two Schottky diodes and two capacitors. At the inital stage of the voltage doubler, the first diode's anode is tied to ground. As the RF input goes negative, the diode becomes forwar biased, allowing charge to flow onto the first capacitor. Once the voltage on the first capacitor is high enough, the second diode turns "on" and begins conducting. This current then flows onto the second capacitor, with twice the voltage as the first (assuming no voltage drop across the diode). This comprises one voltage doubler stage. By cascading additional stages, it is possible to further boost the input voltage.

In practice, this type of voltage doubler — often called a Cockcroft-Walton generator — has a number of drawbacks. When the number of cascaded stages is increased, the voltages of the later

stages begin to sag, primarily due to the AC impedance of the capacitors in the lower stages. And, when supplying an output current, the voltage ripple rapidly increases as the number of stages is increased. For these reasons, CW multipliers with large number of stages are used only where relatively low output current is required [1]. As shown in [2], there is little voltage gain past 40 stages. For this reason, the number of stages is limited to 40 in this design.

3   Design

A variety of voltage doubler circuits have been designed in order to determine what size/type of diodes and what size capacitor performs best. Since the simulation takes a large period of time at such high frequencies and long time periods, it is impractical to simulate each design over a large range of frequencies and input voltages. In lieu of such an indevor, multiple designs were created which will have varying real-world performance. Since this design is intended to be an investigation of RF energy harvesting and more of a proof of concept rather than finished product, performance is not the main focus, rather, it is the concepts and practicality of the design that are being tested. That being said, the following subsectioins describe the design of each doubler stage.

3.1   Voltage Doubler One

The first voltage doubler circuit consists of two p-type Schotty diodes and two high capacity metal-insulator-metal (MIM) capacitors. The diodes each have a width of 5 μm and length of 5 μm. Each capacitor has a width of 25 μm, length of 15 μm, and a total capacitance of $\approx$ 1 pF. A schematic of the doubler can be seen in Figure 1.

3.2   Voltage Doubler Two

The second voltage doubler circuit consists of two p-type Schotty diodes and two high capacity metal-insulator-metal (MIM) capacitors. The diodes each have a width of 5 μm and length of 5 μm. Each capacitor has a width of 30 μm, length of 25 μm, and a total capacitance of $\approx$ 2 pF. A schematic of the doubler can be seen in Figure 2.
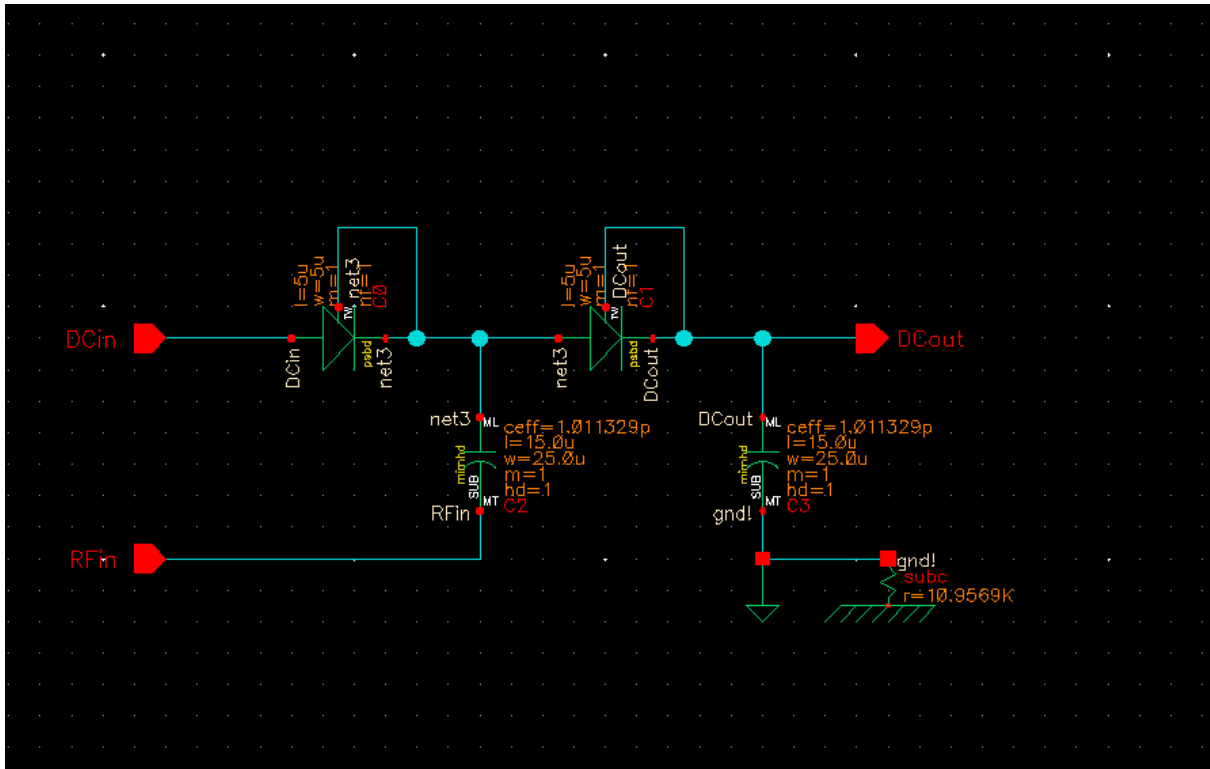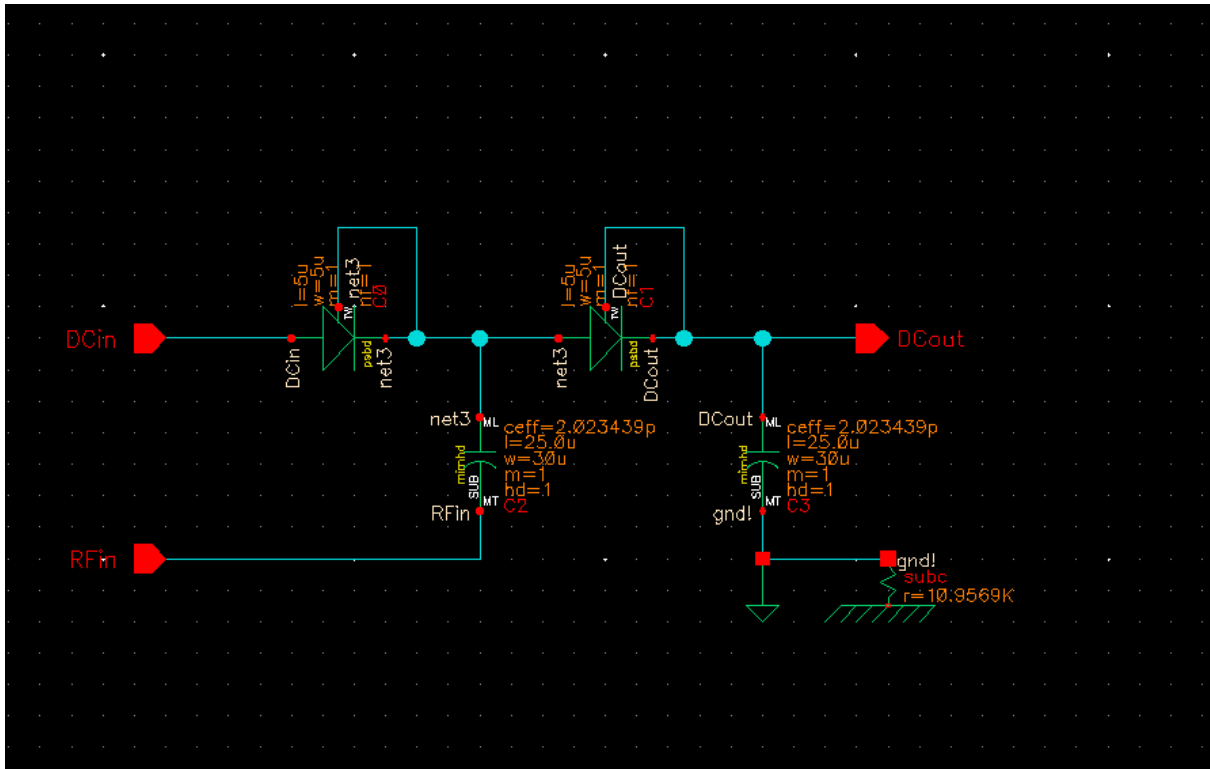
Figure 1: Voltage Doubler 1
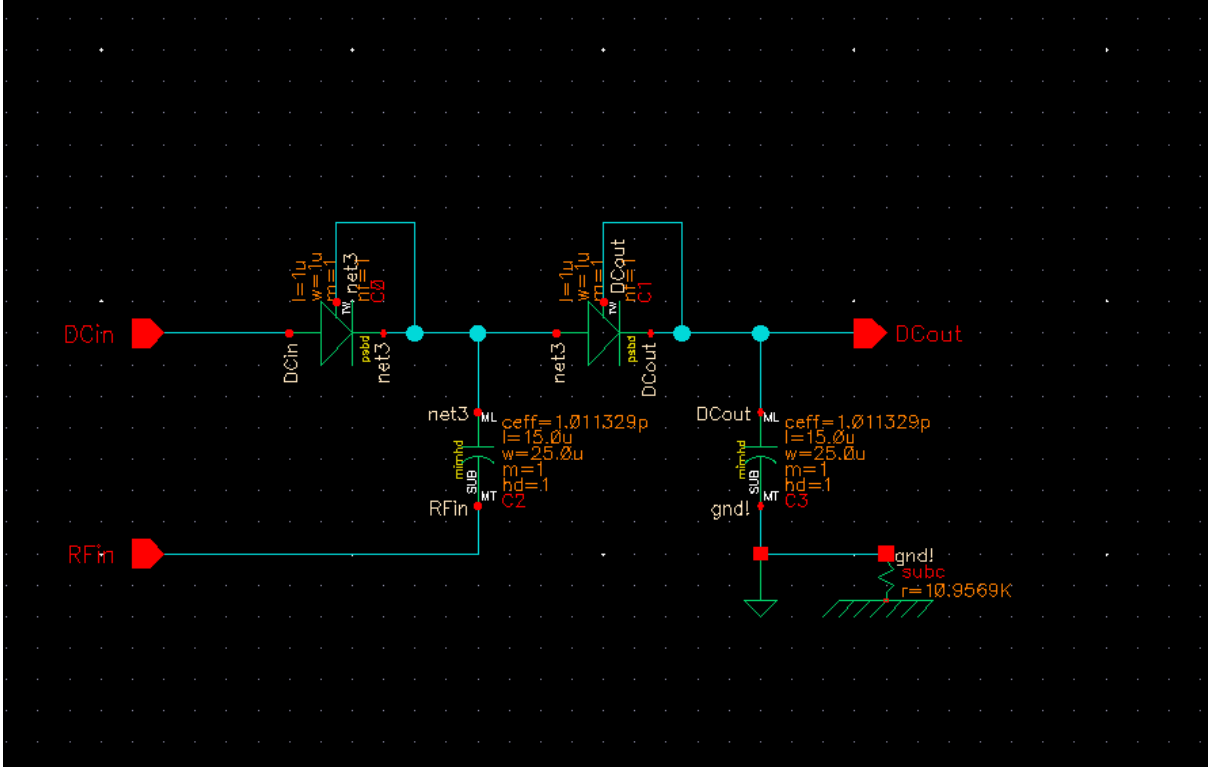
Figure 2: Voltage Doubler 2

Figure 3: Voltage Doubler 3

3.3 Voltage Doubler Three

The third voltage doubler circuit consists of two p-type Schotty diodes and two high capacity metal-insulator-metal (MIM) capacitors. The diodes each have a width of 1 μm and length of 1 μm. Each capacitor has a width of 25 μm, length of 15 μm, and a total capacitance of $\approx$ 1 pF. A schematic of the doubler can be seen in Figure 3.

3.4 Voltage Doubler Four

The fourth voltage doubler circuit consists of two p-type Schotty diodes and two high capacity metal-insulator-metal (MIM) capacitors. The diodes each have a width of 1 μm and length of 1 μm. Each capacitor has a width of 30 μm, length of 25 μm, and a total capacitance of $\approx$ 2 pF. A schematic of the doubler can be seen in Figure 4.
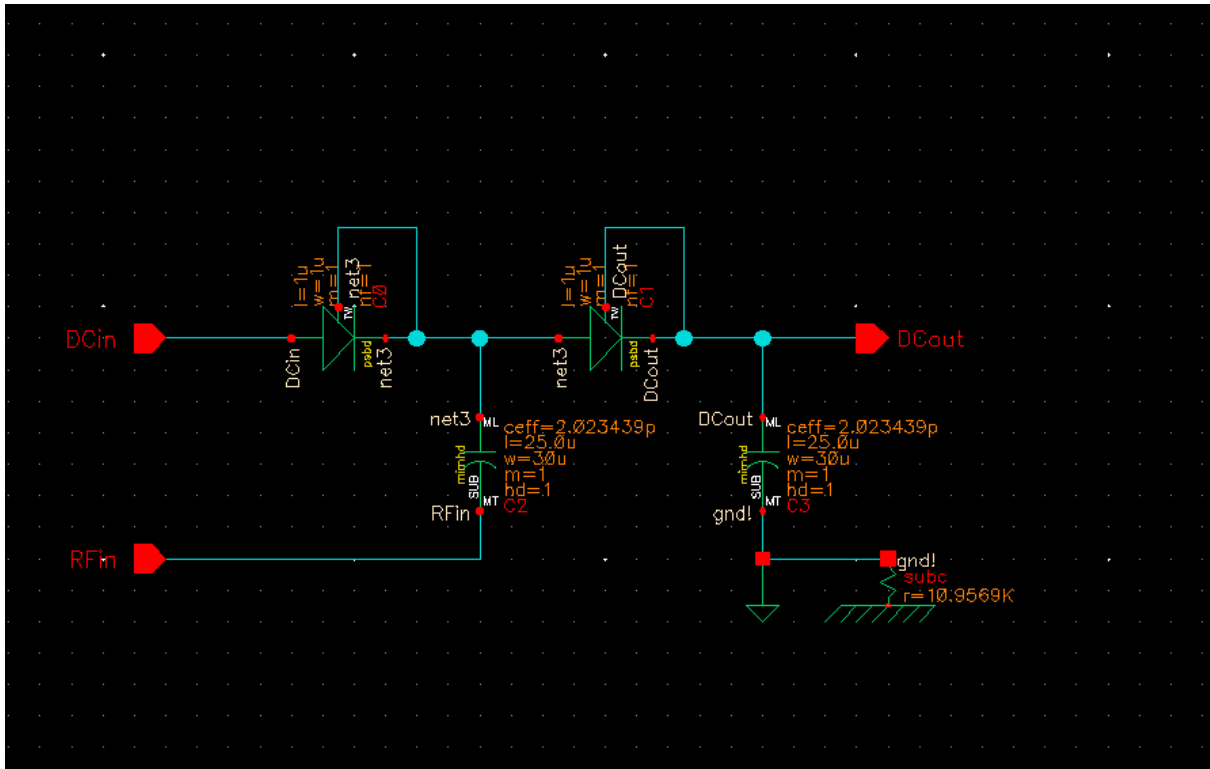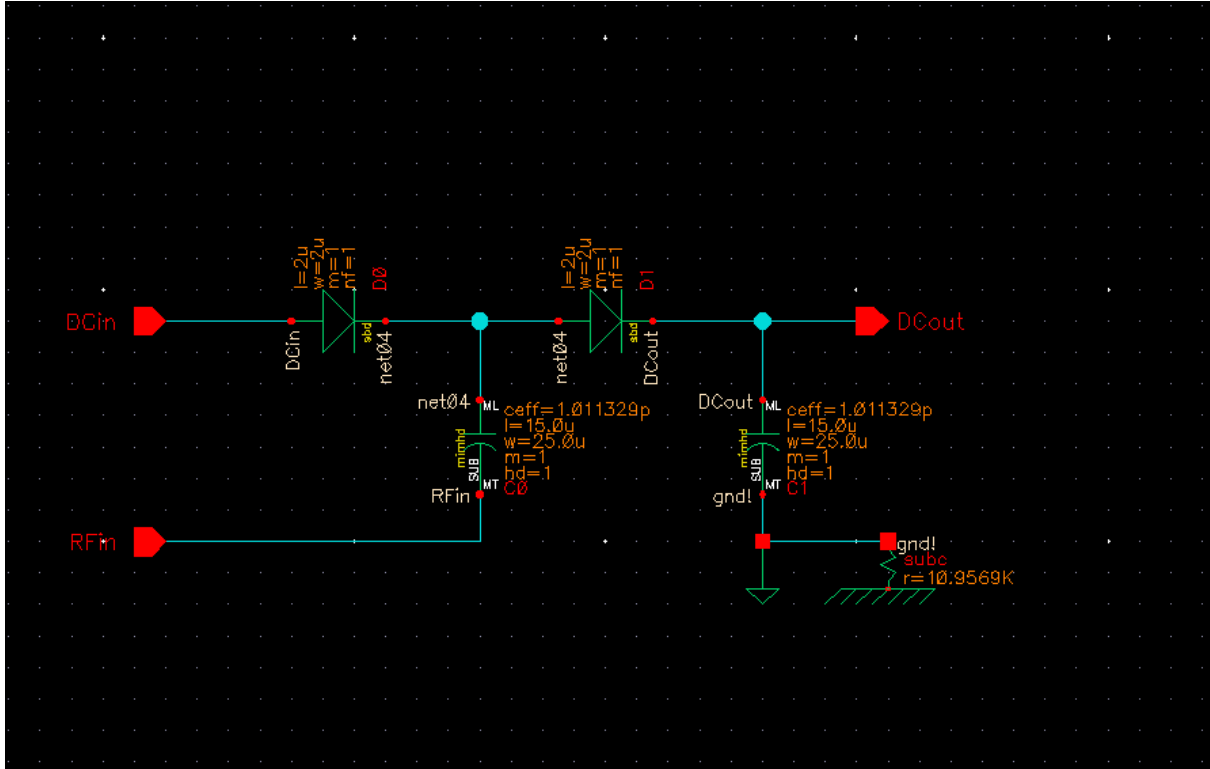
Figure 4: Voltage Doubler 4

Figure 5: Voltage Doubler 5

3.5   Voltage Doubler Five

The fifth voltage doubler circuit consists of two n-type Schotty diodes and two high capacity metal-insulator-metal (MIM) capacitors. The diodes each have a width of 2 μm and length of 2 μm. Each capacitor has a width of 25 μm, length of 15 μm, and a total capacitance of $\approx$ 1 pF. A schematic of the doubler can be seen in Figure 5.

3.6   Voltage Doubler Six

The sixth voltage doubler circuit consists of two n-type Schotty diodes and two high capacity metal-insulator-metal (MIM) capacitors. The diodes each have a width of 1 μm and length of 1 μm. Each capacitor has a width of 25 μm, length of 15 μm, and a total capacitance of $\approx$ 1 pF. A schematic of the doubler can be seen in Figure 6.
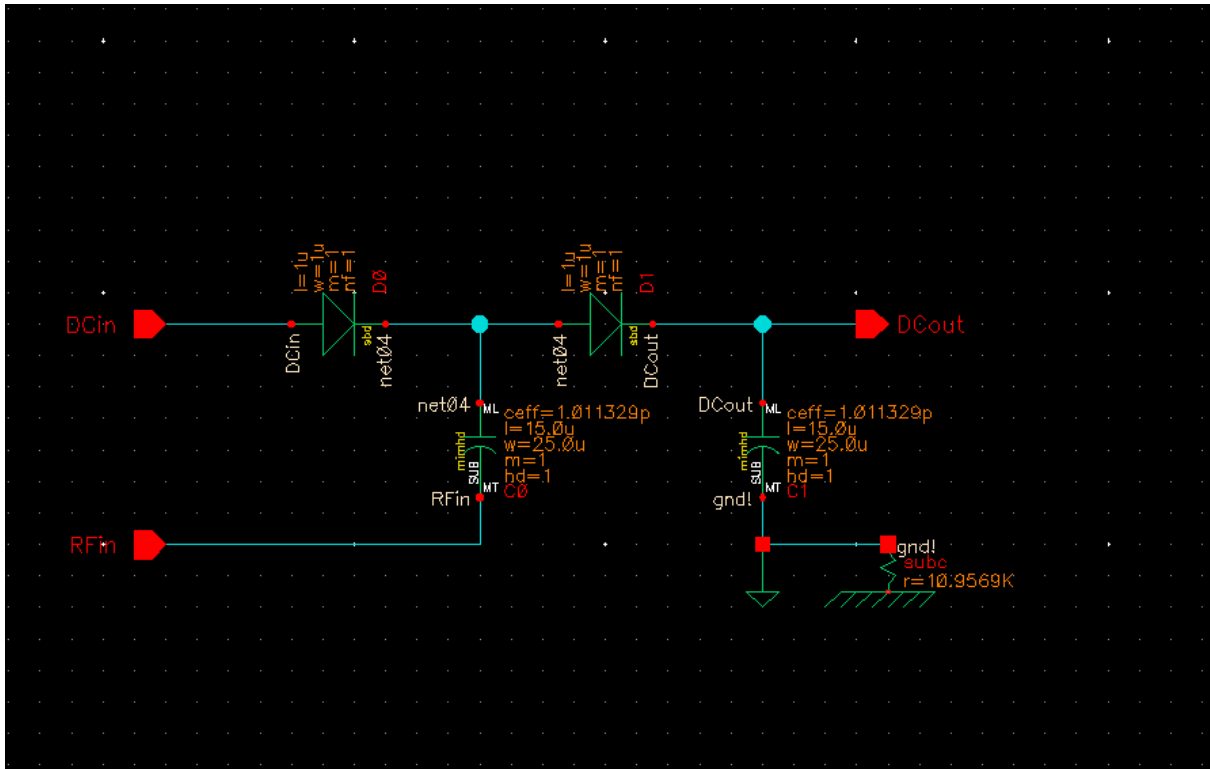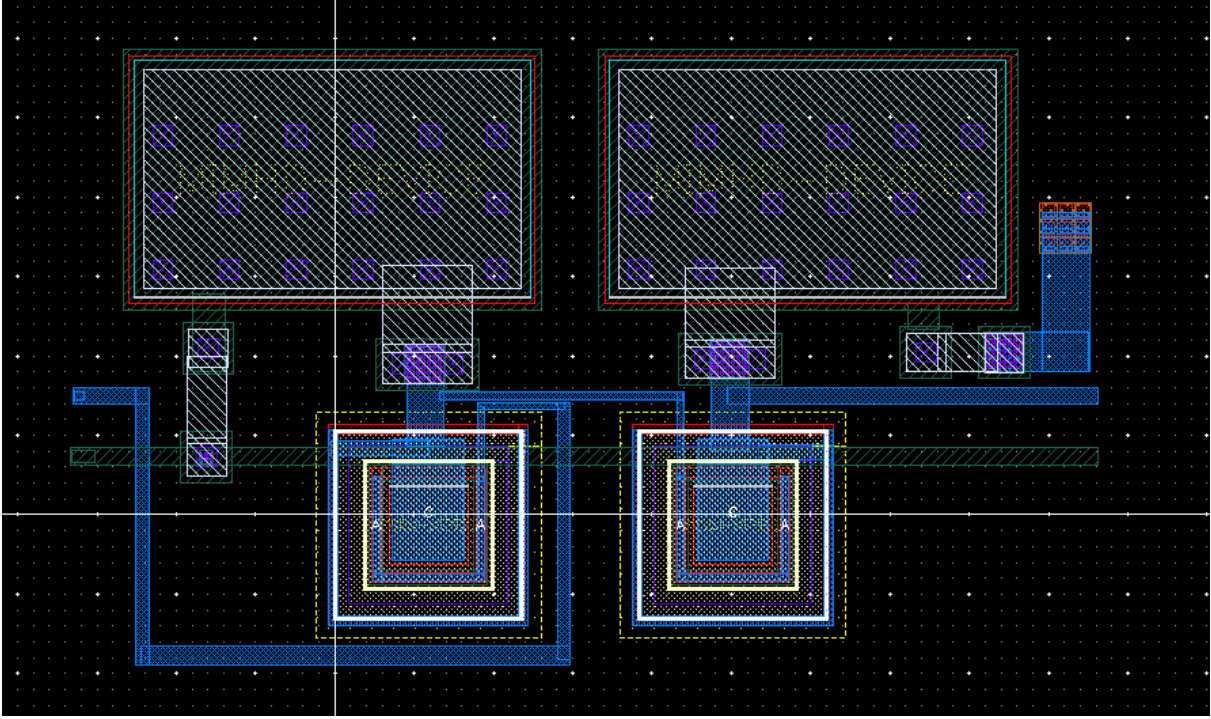
Figure 6: Voltage Doubler 6

Figure 7: Sample layout for a single voltage doubler

4 Layout

Chip layout was done to optimize the density of RF harvester circuits. On average, each doubler is approximately 50 microns in length and 25 mincrons in width. There are 14 total energy harvester circuits which are comprised of a total of 353 individual voltage doublers. Figure 7 shows the layout of voltage doubler 1, consisting of two MIMHD capacitors (each $25\mu m \times 15\ \mu m$) and two p-type Schottky diodes (each $5\mu m \times 5\ \mu m$). Figure 15 shows the complete chip layout.

The layout was optimized in such a way that by creating an instance with multiple columns, there was no need for drawing additional layers of metal to connect each stage of voltage doubler. This allowed space to be saved and also ensured that there would be no defects from stage to stage.

5 Simulation

Due to the large number of circuits and the amount of time required to run realistic simulations, the number of simulations shown in this report has been reduced. The following subsections will show simulations of: one single-stage voltage doubler, one 20 stage RF harvester without extracted
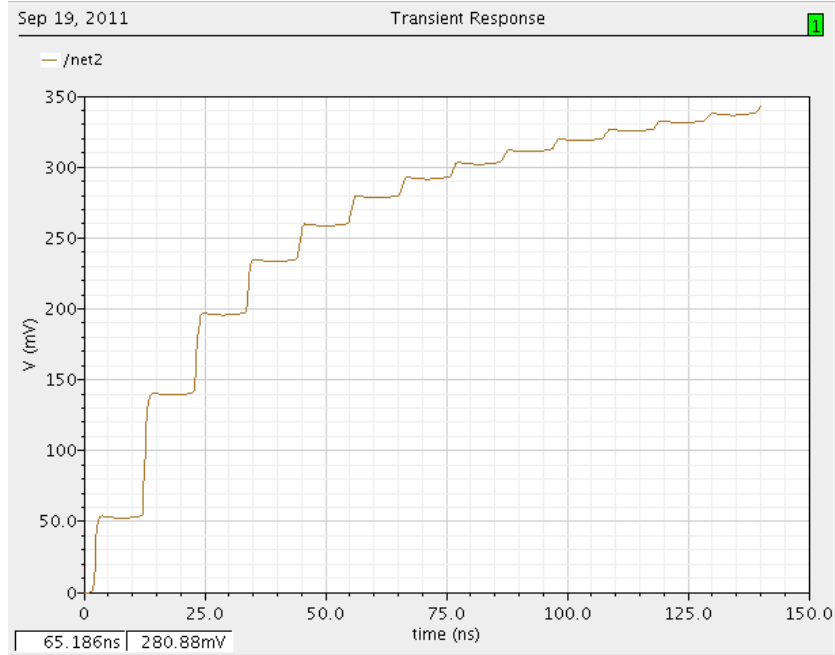
Figure 8: Single-stage voltage doubler with p-type Scottky diodes. 150 mV input signal at 95 MHz

parasitics, one 20 stage n-type harvester without extracted parasitics, one 20 stage RF harvester with extracted parasitics, one 40 stage harvester without extracted parasitics, and one simulation of the top level design using a 40 stage harvester. We will assume that all harvesters are p-type unless otherwise mentioned.

5.1 Single-stage Voltage Doubler

Figure 8 shows an ideal simulation (without extracted parasitics) over a 150 μs time range for a one stage voltage doubler. The input voltage is 150 mV at 95 MHz. The input voltage doubles in roughly 75 ns. The period of a 95 MHz sine wave is

$$\frac{1}{95 \times 10^6} \approx 10 \text{ ns}.$$

We see that at the end of each 10 ns period, the output voltage increases. At first this voltage step is large and as time increases the steps begin to flatten out. When viewed over a longer time period, this appears to be a logrithmic-type curve.
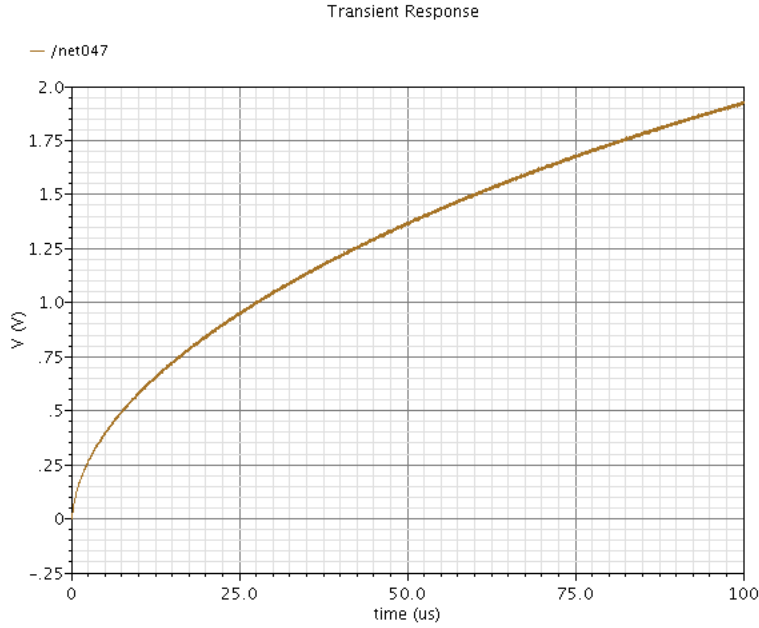
13

Figure 9: 20 Stage RF harvester with 150 mV input signal at 95 MHz.

5.2   20 Stages Ideal

Figure 9 shows an ideal simulation (without extracted parasitics) over a 100 μs time range. The input voltage is 150 mV at 95 MHz and the output voltage is approximately 1.9 V at 100 μs.

5.3   20 Stages Ideal — N-type Diode

Figure 10 shows a 20 stage n-type harvester over a slightly larger time period of 140 μs. This simulation is without extracted parasitics. Note that even with a longer simulation time, the output voltage is not as large as with the p-type Schottky diodes.

5.4   20 Stages Extracted Parasitics

Figure 11 shows the simulation of a 20 stage RF harvester with extracted parasitics of a 100 μs time range. Comparing Figure 9 and Figure 11 we see a slight difference in output voltage, as expected. That is, when factoring in parasitic capacitances between the layers and devices, there is a slight drop is the output voltage. The values seen in Figure 11 will more closely represent the experimental results. At $t = 100$ μs, the difference between the two voltages is approximately 1.9 V $-$ 1.4 V $=$ 0.5 V. It is important to note, however, that the output voltage has not settled
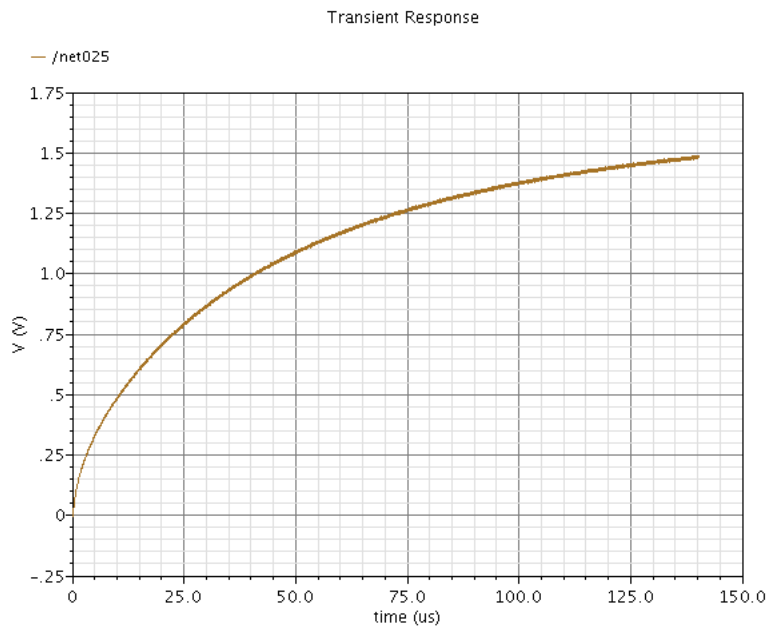
14

Figure 10: 20 Stage n-type RF harvester with 150 mV input signal at 95 MHz.
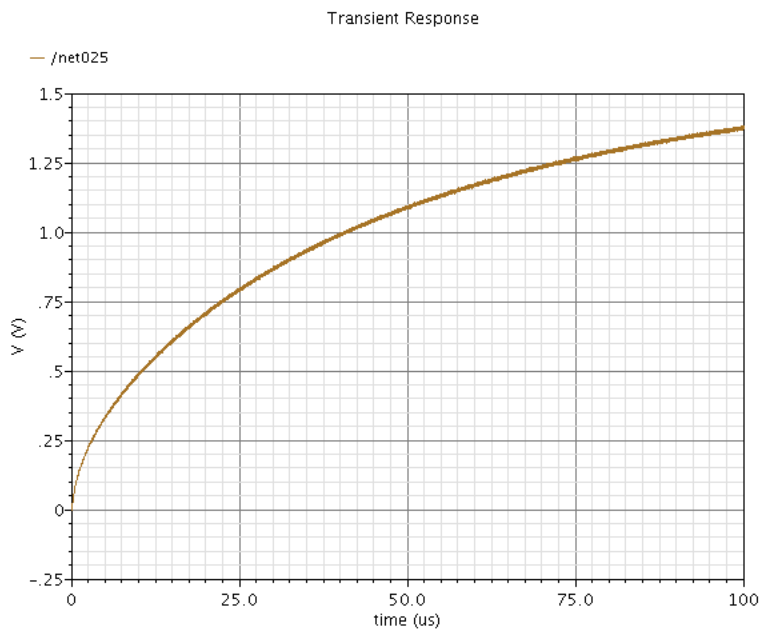

Figure 11: 20 Stage RF harvester with 150 mV input signal at 95 MHz and extracted parasitics.
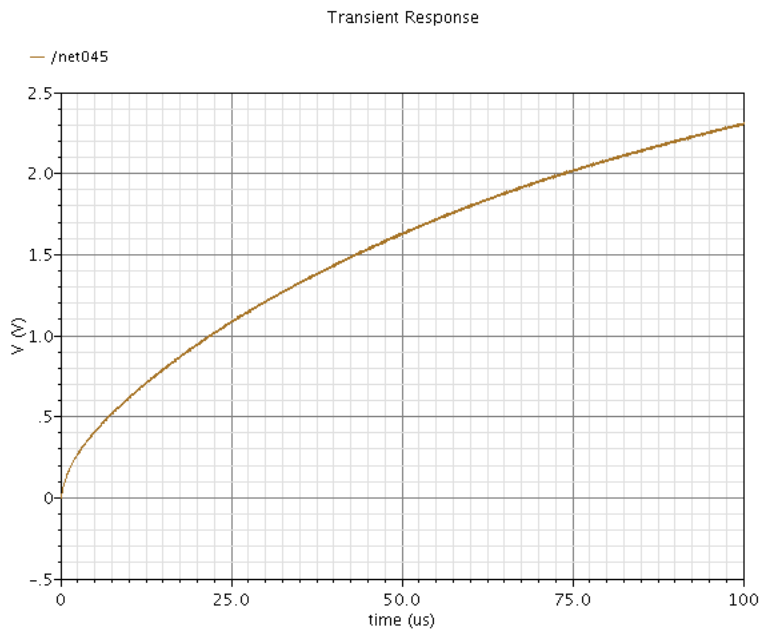
Figure 12: 40 Stage RF harvester with 150 mV input signal at 95 MHz.

over the 100 μs period, meaning the voltage would continue to increase with greater t.

5.5   40 Stages Ideal

Figure 12 shows the simulation of a 40 stage RF harvester, without extracted parasitics. Compared to Figure 9, there is a significant increase in output voltage over the same time period, with the same input source. This proves that cascading more stages produces a higher output voltage. Both simulations are run with voltage doubler two.

5.6   40 Stages — Top Level Chip

Figure 13 shows the schematic for the complete test setup. The input source was again 150 mV at 95 MHz. Output load capacitance was 1 pF. Unused pins are grounded.

6   Analysis

Simulations show that on average, an output voltage of 1.75 V is acheived after 100 μs. Since the slope voltage vs. time curve is still fairly large at the end of this time period, the output voltage
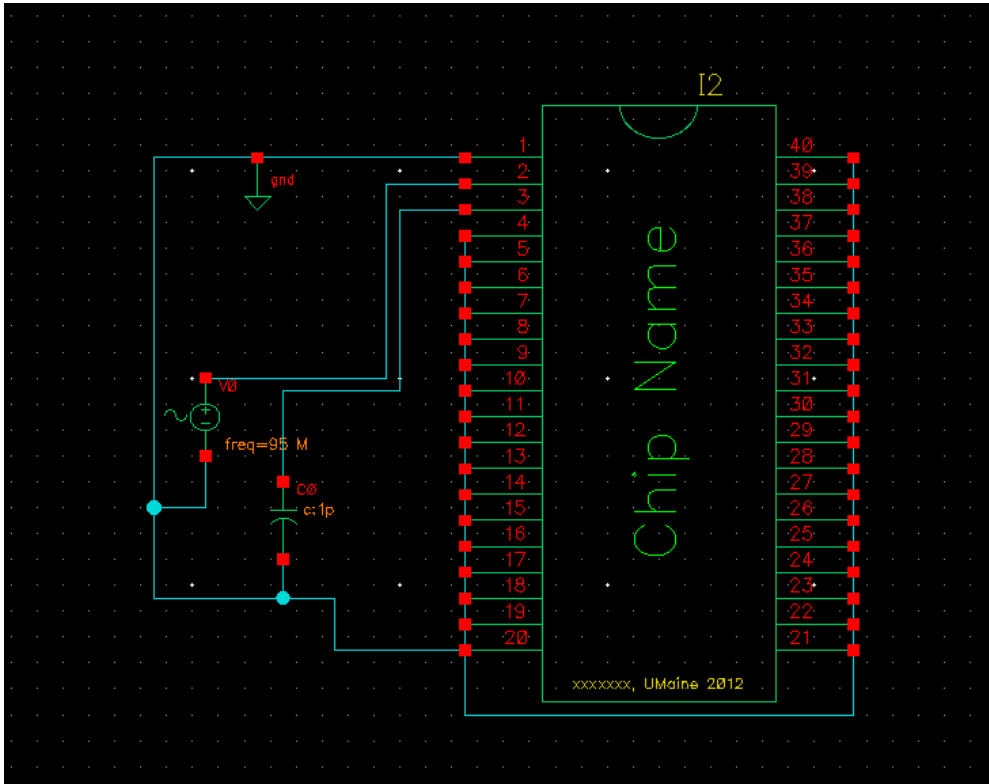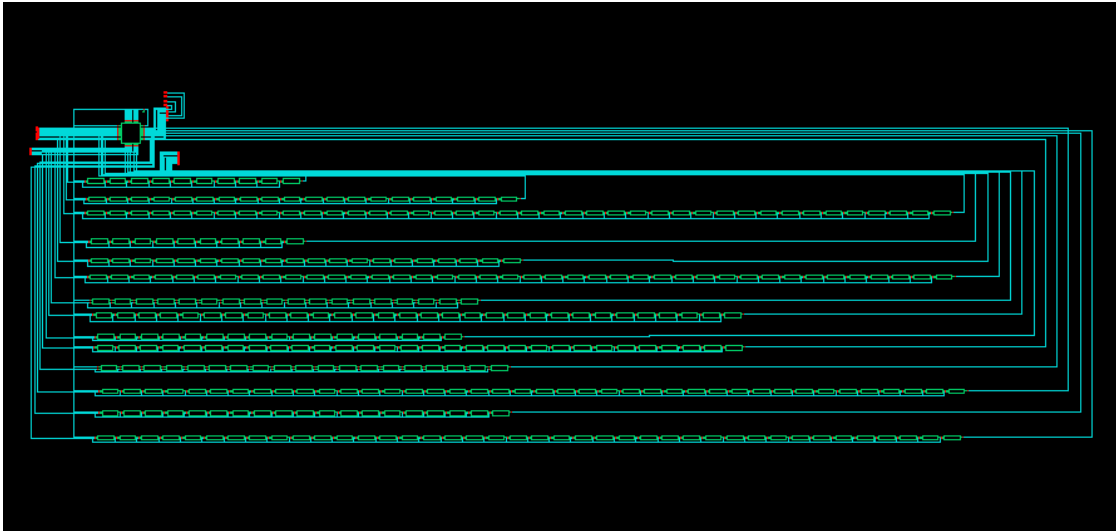
16

Figure 13: Test schematic

Figure 14: Top-level schematic

17

would increase even greater after 100 μs. If we extrapolate the curve of Figure 9 for example, we can see that we would reach an output voltage of approximately 4 to 5 V as $t \rightarrow \infty$. Under real world circumstances, the voltages seen at the output would be significantly higher than what the simulations indicate because of the longer time periods involved. Lab measurements could potentially indicate up to 5 V outputs.

We also see that the type of diode used does affect the performance of the circuit. The n-type diode of Figure 10 does not perform as well as the p-type diode of Figure 9, even though the n-type harvester simulated for 40 μs more. This is presumably because of the higher turn on voltage of the n-type (≈ 3 V) compared to the p-type (≈ 1.1 V). The higher turn on voltage means that the built in potential of the metal semiconductor contact is reducing the voltage seen at the output.

In general, we see that the larger stage p-type harvesters performed better. Since we are only looking at the output voltage, however, we may potentially see that the smaller stage harvesters are able to source more current or perhaps have a higher energy density. Experimental testing of the design will further explore this.

7   Verification

The chip layout and connections have been varified using DRC, LVS, Pattern density, local pattern density, and floating gate checks. The checks indicate that there are no problems with the layout (DRC) or with the correlation between layout and schematic (LVS). These results indicate that the design is ready to be sent to fabrication. Figure 15 shows the complete chip layout.

8   Conclusion

This report presents the design and simulation of various energy harvester circuits. The overall design consists of six different "voltage doubler" configurations. From the six configurations, 14 independent energy harvester circuits have been designed, each consisting of various series connections of the voltage doublers. Simulations with a 150 mV 90 MHz input signal indicate an average output voltage of 1.75 V over a 100 μs time scale for 10 cascaded voltage doublers. For 40 stages in series, the output voltage improves to over 2 V over the same 100 μs range. Simulations prove that
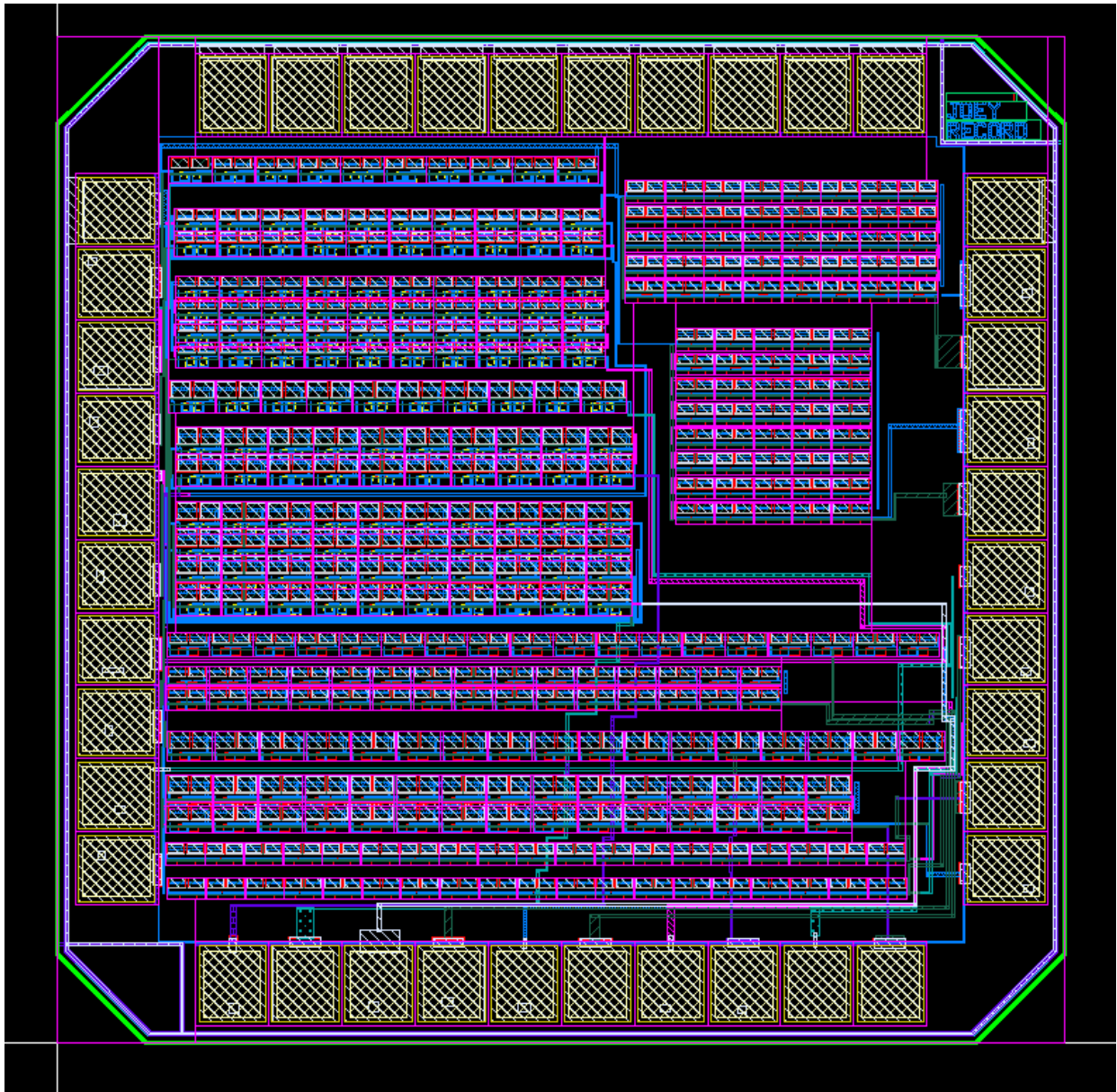
Figure 15: Complete chip layout

more stages provide a higher output voltage. In general, n-type Schottky diodes performed better than their p-type Schottky counterparts, largely because of the n-type's lower turn on voltage.

Future improvements could include changing the capacitance at each stage, such that the first stages have higher value of capacitance. This would reduce potential ripple on the output and allow greater currents to be sourced. Also, pn-junction doides could be experimented with at the later stages to reduce potential reverse leakage current of the Schottky diodes.

References

[1] Wikipedia. *Cockcroft-Walton Generator.*

http://en.wikipedia.org/wiki/Cockcroft-Walton_generator

[2] Le *et al.*. "Efficient far-field radio frequency energy harvesting for passively powered sensor networks." *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 5, May 2008.